Daffodil International University

Department of Software Engineering
Faculty of Science & Information Technology
Midterm Examination, Spring 2025
Course Code: SE 222; Course Title: Computer Architecture
Batch & Sections: 42 (A, B, C, D, E, F, G, H, I, J K)
Course Teachers: SP (A, D, E, F,), KBB (B, C, G), FC (J), HKN (H, I), AAS (K)

Time: 1 Hour 30 Mins **Marks:25**

Answer ALL Questions

[The figures in the right margin indicate the full marks and corresponding course outcomes. All portions of each question must be answered sequentially.]

1. a) A processor has base clock speed of 1.2 GHz. It is used to execute a benchmark program with the following instruction mix and clock cycle count. **[Marks-6]** **CLO1 Level 2**

Instruction Type	Instruction Count	Clock Cycle Count
Arithmetic	42000	1
Data Transfer	35000	2
Floating Point	18000	3
Control Transfer	5000	2

Determine the effective CPI, MIPS rate and execution time for this program.

b) Suppose that a task makes extensive use of floating-point operations, with 60% of the time is consumed by floating-point operations. With a new hardware design, the floating-point module is speeded up by a factor of 6. **Compute** the overall speedup. **[Marks-2]**

c) **Describe** a general-purpose processor along with diagram. **[Marks-4]**

d) **Explain** an interrupt cycle with proper diagram. **[Marks-3]**

2.a) **[Marks-5]** **CLO2 Level 2**

Memory	
300	1941
301	C942
302	2942
941	0004
942	0002

CPU Register	
300	PC
	AC
	IR

Here memory contents are represented in hexadecimal:
0001---Load AC from Memory
1100---Subtract AC from Memory
0010---Store AC to Memory Location

Where A=10, B=11, C=12, D=13, E=14, F =15
Explain the program execution steps for the given scenario.

b) **Visualize** a three-level cache organization. **[Marks-2]**

c) **Classify** the types of performance parameters of memory and elaborate the relationship for non-random access memory in terms of times. **[Marks-3]**