Daffodil International University

Faculty of Science & Information Technology

Final Examination, Spring 2023

Course Code: CSE411

Course Title: Computer Architecture and Organization

Level: 4 Term: 1 Batch: 56

Time: 2 Hours **Marks: 40**

Answer ALL Questions

[The figures in the right margin indicate the full marks and corresponding course outcomes. All portions of each question must be answered sequentially.]

1.	a)	**Assume** a direct mapped cache with a block size of 4 KB. The size of the main memory is 16 GB and there are 10 bits in the tag. Find the Size of cache memory and calculate the logical and physical address for this mapping. **Analyze** the drawbacks of direct mapping.	[8]	CO4
	b)	**List** the parameters considered to measure the performance of memory. As one goes down the hierarchy, **Analyze** the change in cost per bit, capacity, access time, and frequency of access of the memory by the processor.	[4]	
2.	a)	**Demonstrate** the diagram of the multiplier which is used for fixed point multiplication of 5*5 unsigned binary numbers.	[4]	CO2
	b)	In computer architecture, the pipeline is a fundamental concept for improving CPU performance. Considering the basic structure of a pipeline, assuming that you are working with 5 bits number, **Explain** the basic structure of a pipeline in a CPU and the purpose of each stage.	[4]	
3.	a)	The pipeline has a five-stage structure: Instruction Fetch (IF), Instruction Decode (ID), Execute (EX), Memory Access (MEM), and Write Back (WB). The processor encounters a control hazard in the form of a conditional branch instruction. The control hazard introduces a pipeline stall of three cycles, during which no new instructions can enter the pipeline. Assume that the pipeline encounters a control hazard at cycle 25, and the branch instruction takes a total of five cycles to complete. **Construct** the timing diagram, at which the pipeline can resume its normal execution flow without any additional stalls, considering the control hazard and the required cycles for the branch instruction.	[5]	CO
	b)	A non-pipeline system takes 50 ns to process a task. The same task can be processed in a six segments pipeline with a clock cycle of 10 ns. **Identify** the speedup ratio of the pipeline for 100 tasks.	[4]	
4.	a)	You are a system administrator for a company that runs a high-traffic e-commerce website. The website experiences a significant increase in traffic during seasonal sales events, causing performance issues due to limited physical memory on the servers. To address this, **Analyze** the technique will you follow.	[4]	CO4
	b)	For the above question, the operating system runs on a server that hosts multiple applications simultaneously. To optimize memory utilization, you are exploring the concept of memory sharing in virtual memory. **List** its benefits and potential challenges.	[4]	
	c)	**Analyze** the process of address translation with proper diagrams	[3]	