



Daffodil International University

Faculty of Science & Information Technology

Department of Software Engineering

Midterm Examination, Spring 2026

Course Code: SE222; Course Title: Computer Architecture

Sections & Teachers: 44A to 44K (AS, HKN, HT, AJE)

Time: 1 Hour 30 Mins

Marks: 25

Answer **ALL** Questions

[The figures in the right margin indicate the full marks and corresponding course outcomes. All portions of each question must be answered sequentially.]

1.	a)	A 2 GHz processor was used to execute on a program with the following instruction mix and clock cycle counts: <table><tr><th>Instruction Type</th><th>Frequency</th><th>CPI</th></tr><tr><td>Integer ALU operation</td><td>10%</td><td>1</td></tr><tr><td>Floating point Operation</td><td>40%</td><td>7</td></tr><tr><td>Loads & Stores</td><td>30%</td><td>5</td></tr><tr><td>Branches</td><td>20%</td><td>3</td></tr></table> Compute the effective CPI, MIPS rate and Execution Time for this program.	Instruction Type	Frequency	CPI	Integer ALU operation	10%	1	Floating point Operation	40%	7	Loads & Stores	30%	5	Branches	20%	3	[Marks-5]	CLO-1 Level-2																									
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	b)	Explain Moore's Law and its significance for processor performance. Then, using the exponential growth model, calculate how many transistors a processor will have after 8 years if it initially contains 2 million transistors and the doubling time is 2 years.	[Marks-4]																																									
	c)	Clarify the fetch and execute instruction of GP processor along with diagram.	[Marks-3]																																									
	d)	Suppose that a task makes extensive use of floating-point operations, with 45% of the time is consumed by floating-point operations. With a new hardware design, the floating-point module is speedup by a factor of 12. Compute the speedup using Amdahl's Law.	[Marks-3]																																									
2.	a)	Explain the execution steps of Hypothetical Processor for the given scenario. <table><tr><th colspan="2">Memory</th><th colspan="2">CPU Register</th></tr><tr><td>101</td><td>3606</td><td>101</td><td>PC</td></tr><tr><td>102</td><td>6607</td><td></td><td>AC</td></tr><tr><td>103</td><td>7608</td><td></td><td>IR</td></tr><tr><td>104</td><td>4609</td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td></tr><tr><td>606</td><td>000A</td><td></td><td></td></tr><tr><td>607</td><td>0005</td><td></td><td></td></tr><tr><td>608</td><td>000C</td><td></td><td></td></tr><tr><td>609</td><td>0000</td><td></td><td></td></tr></table> Here memory contents are represented in hexadecimal 0011---Load AC from Memory 0110---Subtract AC from Memory 0100---Store AC to Memory Location 0111---Multiply AC to memory	Memory		CPU Register		101	3606	101	PC	102	6607		AC	103	7608		IR	104	4609							606	000A			607	0005			608	000C			609	0000			[Marks-4]	CLO-2 Level-4
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	b)	Explain the concept of an interrupt handler in a computer system. Describe the steps that occur from the moment an interrupt is generated until the CPU resumes the interrupted program.	[Marks-3]																																									
	c)	Demonstrate the cache read operational diagram of computer system.	[Marks-3]																																									

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