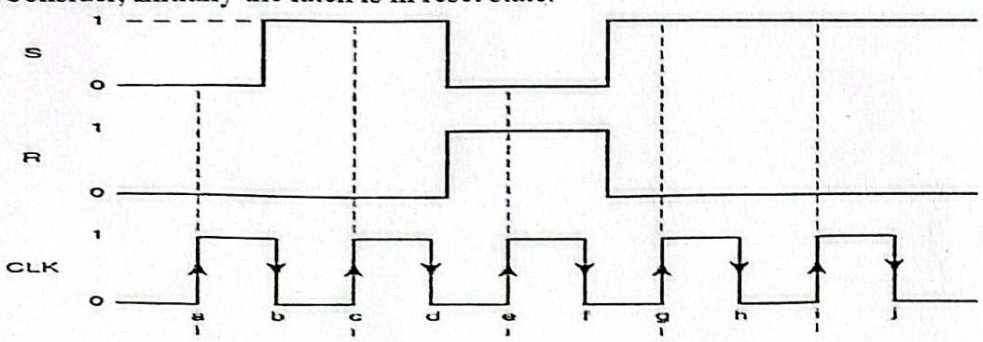
Daffodil International University

Faculty of Science & Information Technology
Department of Computer Science & Engineering
Final Semester Examination, Spring 2026
Course Code: CSE223, Course Title: Digital Logic Design
Level: 2 Term: 2 Batch: 67

Time: 2:00 Hrs **Marks: 40**

[The figures in the right margin indicate the full marks and corresponding course outcomes. Answer all questions. All portions of each question must be answered sequentially.]

1.	a)	In a simple digital processing unit, arithmetic operations are performed using basic combinational building blocks. You are assigned to design a circuit that performs binary addition of two bits along with an input carry. To simplify hardware design, only a 3-to-8 decoder is available in the system. Design a full adder using a decoder.	5	CO3
	b)	The priority levels of four inputs of a 4 to 2 priority encoder are given by w0 > w2 > w1> w3. Using truth table and logic equations, design the logic circuit for priority encoder.	5	
	c)	Apply the Boolean function F (A, B, C, D) = Σ (1, 3, 5, 7, 9, 11, 12, 15) with a Multiplexer. Assume A, B and D are connected with selection lines.	5	
2.	a)	For the following input draw the output waveforms Q & Q' for a SR latch. Consider, Initially the latch is in reset state. 	5	CO4
	b)	Explain the differences between synchronous and Asynchronous counters	5	
3.	a)	A 4-bit Parallel-In Serial-Out (PISO) shift register has a control input S where S = 1 enables parallel loading and S = 0 enables shifting. The register is initially cleared. At the first clock pulse, the input $D_3D_2D_1D_0$ = 1011 is applied with S = 1, and for the next clock pulses S = 0 is maintained. Explain the operation of the PISO shift register and determine the serial output sequence for the next four clock pulses, assuming right shift with MSB shifted out first.	5	CO4
	b)	Design a MOD-7 synchronous up counter with proper diagrams and tables and briefly explain the counting sequence.	5	
	c)	Explain the working principle of a JK flip-flop with a neat diagram. Also mention how it eliminates the race condition.	5	