Daffodil International University

Faculty of Science & Information Technology

Department of Software Engineering

Midterm Examination, Summer 2026

Course Code: SE222; Course Title: Computer Architecture

Sections & Teachers: 45A to 45L (MH, KBB, HKN, FC)

Time: 1 Hour 30 Mins **Marks: 25**

Answer ALL Questions

[The figures in the right margin indicate the full marks and corresponding course outcomes. All portions of each question must be answered sequentially.]

1. *a)* A processor operates at 1.8 GHz with the following instruction mix: [Marks-5] CLO-1 *Level-2*

Instruction Type	Frequency	CPI
ALU Operation	25%	1
Floating Point	20%	9
Memory Access	35%	4
Branch	20%	3

Compute the effective CPI, MIPS rate, and Execution Time for a program containing 10 million instructions.

b) **Explain** the function of a General Purpose Processor (GPP) and its instruction patterns with a suitable diagram. [Marks-4]

c) **Differentiate** the program flow of control without interrupts and with interrupts in a computer system with suitable diagrams. [Marks-3]

d) A database server spends 40% of its execution time on disk I/O operations. A new SSD upgrade makes the disk I/O portion 6 times faster. **Analyze** the overall system speedup using Amdahl's Law and state whether the upgrade provides a significant performance gain. [Marks-3]

2. *a)* **Analyze** the execution steps of the Hypothetical Processor for the given scenario. [Marks-4] CLO-2 *Level-4*

Memory		CPU Register	
400	1808	PC	400
401	6809	AC	0000
402	580A	IR	—
403	480B		

Here memory contents are represented in hexadecimal

808	0012	
809	0006	
80A	0004	
80B	0000	

Opcode: 0001—Load AC from Memory, 0110—Add AC from Memory, 0101—Subtract AC from Memory, 0100—Store AC to Memory

	b)	**Distinguish** between the levels of the memory hierarchy in terms of speed, cost, and capacity, and why using a single large fast memory is impractical for modern computer systems.	[Marks-3]	
	c)	**Examine** the role of tag, line, and word fields in cache address decomposition and how the processor determines a cache hit or miss during a memory read operation.	[Marks-3]	