CPU Performance

1. CPU performance is primarily measured by
A. CPU size
B. Execution time
C. Clock cycle length
D. Power consumption
Answer: B
2. Which factor directly affects CPU performance?
A. Number of registers
B. Clock speed
C. Monitor resolution
D. Keyboard speed
Answer: B
3. CPU performance can be increased by
A. Increasing execution time
B. Decreasing clock rate
C. Increasing clock rate
D. Reducing cache memory
Answer: C
4. CPU performance is inversely proportional to
A. Clock rate
B. CPI
C. Execution time
D. Instruction count
Answer: C
5. Which equation represents CPU execution time?
A. Instruction Count × CPI × Clock Cycle Time
B. CPI ÷ Clock Rate
C. Clock Rate ÷ Instruction Count
D. Execution Time × CPI
Answer: A
6. CPI stands for
A. Cycles Per Instruction
B. Cost Per Instruction
C. Cycles Per Interrupt
D. Clock Performance Index
Answer: A
7. Lower CPI indicates
A. Slower CPU
B. Better performance
C. Higher power usage
D. Larger instruction set
Answer: B
8. Which unit measures clock speed?
A. Bytes
B. Hertz
C. Seconds
D. Joules
Answer: B
9. Increasing cache size generally

A. Decreases performance
B. Has no effect
C. Improves performance
D. Increases CPI
Answer: C
10. Which memory is fastest?
A. RAM
B. Cache
C. Hard disk
D. ROM
Answer: B
11. CPU performance is affected by
A. Instruction count
B. CPI
C. Clock rate
D. All of the above
Answer: D
12. A higher clock rate always means better performance
A. True
B. False
Answer: B
13. Which component reduces average memory access time?
A. Hard disk
B. Cache memory
C. Virtual memory
D. Secondary storage
Answer: B
14. Pipelining improves CPU performance by
A. Increasing CPI
B. Executing instructions sequentially
C. Overlapping instruction execution
D. Reducing clock speed
Answer: C
15. Which technique increases instruction throughput?
A. Paging
B. Pipelining
C. Swapping
D. Fragmentation
Answer: B
16. Speedup due to pipelining is ideally equal to
A. Number of pipeline stages
B. CPI
C. Clock rate
D. Instruction count
Answer: A
17. Amdahl's Law relates to
A. Memory hierarchy
B. CPU cost
C. Performance improvement
D. Power consumption
Answer: C
18. Which factor limits maximum speedup?

A. Clock speed
B. Parallelizable portion
C. Serial portion
D. Cache size
Answer: C
19. Multicore processors improve performance by
A. Increasing clock speed
B. Reducing instruction size
C. Parallel execution
D. Increasing power usage
Answer: C
20. Throughput refers to
A. Time to execute one instruction
B. Number of instructions per second
C. Clock cycle time
D. CPI
Answer: B
21. Latency refers to
A. Instruction count
B. Total execution time
C. Instructions per second
D. Cache hit rate
Answer: B
22. Which factor does NOT affect CPU performance?
A. Compiler optimization
B. Instruction set architecture
C. Hard disk capacity
D. Cache size
Answer: C
23. RISC processors usually have
A. High CPI
B. Complex instructions
C. Simple instructions
D. Large instruction size
Answer: C
24. CISC processors aim to
A. Reduce instruction complexity
B. Reduce instruction count
C. Increase CPI
D. Increase clock cycle time
Answer: B
25. Which improves performance without increasing clock speed?
A. Overclocking
B. Pipelining
C. Increasing execution time
D. Reducing cache
Answer: B
26. Cache hit ratio affects
A. Clock speed
B. Memory access time
C. Power consumption
D. Instruction size

Answer: B
27. The performance of a CPU is improved by
A. Increasing CPI
B. Increasing instruction count
C. Reducing execution time
D. Reducing clock speed
Answer: C
28. Which is a performance metric?
A. MIPS
B. RAM size
C. Disk speed
D. Screen resolution
Answer: A
29. MIPS stands for
A. Mega Instructions Per Second
B. Million Instructions Per Second
C. Memory Instructions Per Second
D. Machine Instructions Per Second
Answer: B
30. Which is NOT a reliable performance metric?
A. Execution time
B. CPI
C. MIPS
D. Clock cycle time
Answer: C
31. Which memory hierarchy level has lowest latency?
A. Registers
B. Cache
C. Main memory
D. Secondary storage
Answer: A
32. Branch prediction improves
A. Cache size
B. Pipeline efficiency
C. Clock rate
D. Instruction size
Answer: B
33. Which causes pipeline stalls?
A. Data hazards
B. Control hazards
C. Structural hazards
D. All of the above
Answer: D
34. Superscalar processors improve performance by
A. Executing one instruction at a time
B. Increasing clock cycle
C. Executing multiple instructions per cycle
D. Reducing cache
Answer: C
35. Which factor increases CPI?
A. Cache misses
B. Pipelining

C. Branch prediction
D. Compiler optimization
Answer: A
36. Which improves CPU utilization?
A. Multithreading
B. Paging
C. Swapping
D. Fragmentation
Answer: A
37. Execution time decreases when
A. CPI increases
B. Clock cycle time decreases
C. Instruction count increases
D. Cache size decreases
Answer: B
38. Which is a static performance metric?
A. Execution time
B. Clock rate
C. Throughput
D. Latency
Answer: B
39. Which metric is user-oriented?
A. CPI
B. Clock rate
C. Execution time
D. Cache hit rate
Answer: C
40. Which improves instruction-level parallelism?
A. Pipelining
B. Branching
C. Paging
D. Segmentation
Answer: A
41. Moore's Law relates to
A. Performance scaling
B. Transistor count growth
C. Clock speed
D. Power efficiency
Answer: B
42. Increasing pipeline depth may
A. Reduce hazards
B. Increase clock speed
C. Increase branch penalty
D. Reduce throughput
Answer: C
43. Which metric compares different architectures fairly?
A. Clock speed
B. MIPS
C. Execution time
D. CPI
Answer: C
44. CPU-bound programs are limited by

A. Disk speed
B. Network speed
C. CPU performance
D. Memory capacity
Answer: C
45. Which improves performance per watt?
A. Overclocking
B. Multicore design
C. Increasing voltage
D. Increasing CPI
Answer: B
46. SIMD improves performance by
A. Executing different instructions
B. Executing same instruction on multiple data
C. Increasing clock rate
D. Reducing cache
Answer: B
47. Which causes performance degradation?
A. Cache hits
B. Pipeline stalls
C. Branch prediction
D. Parallel execution
Answer: B
48. Which is NOT part of CPU performance equation?
A. Instruction count
B. CPI
C. Clock cycle time
D. Cache size
Answer: D

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49. Increasing instruction count will
A. Increase performance
B. Reduce execution time
C. Increase execution time
D. Reduce CPI
Answer: C
50. Which technology improves CPU performance by hiding latency?
A. Multithreading
B. Paging
C. Swapping
D. Fragmentation
Answer: A
51. CPU performance is best evaluated using
A. Synthetic benchmarks
B. Real-world workloads
C. Clock speed
D. MIPS
Answer: B
52. Which benchmark measures integer performance?
A. SPECint
B. SPECfp

C. LINPACK
D. TPC
Answer: A
53. Floating-point performance is measured by
A. SPECint
B. SPECfp
C. MIPS
D. CPI
Answer: B
54. Which factor improves cache performance?
A. Higher miss rate
B. Better locality
C. Larger instruction count
D. Slower memory
Answer: B
55. Temporal locality means
A. Accessing nearby memory locations
B. Reusing the same data
C. Sequential execution
D. Parallel execution
Answer: B
56. Spatial locality means
A. Reusing same instruction
B. Accessing nearby memory locations
C. Multithreading
D. Branch prediction
Answer: B
57. Which CPU design focuses on power efficiency?
A. Superscalar
B. VLIW
C. RISC
D. Out-of-order execution
Answer: C
58. Which increases instruction throughput the most?
A. Higher CPI
B. Lower clock rate
C. Parallel execution
D. Larger execution time
Answer: C
59. Performance per dollar refers to
A. Cost efficiency
B. Clock speed
C. Power usage
D. CPI
Answer: A
60. Which statement is correct?
A. Faster clock always means faster CPU
B. Performance depends on multiple factors
C. CPI alone defines performance
D. Cache has no impact
Answer: B

DMA (Direct Memory Access)

1. DMA stands for
A. Direct Memory Allocation
B. Direct Machine Access
C. Direct Memory Access
D. Data Memory Access
Answer: C
2. The primary purpose of DMA is to
A. Increase CPU clock speed
B. Reduce CPU involvement in data transfer
C. Increase memory size
D. Improve cache performance
Answer: B
3. DMA allows data transfer between
A. CPU and registers
B. I/O devices and main memory
C. Cache and registers
D. Secondary storage only
Answer: B
4. Which component controls DMA operations?
A. CPU
B. Cache controller
C. DMA controller
D. Memory controller
Answer: C
5. DMA is mainly used for
A. Small data transfers
B. Large block data transfers
C. Arithmetic operations
D. Instruction execution
Answer: B
6. In DMA, the CPU
A. Transfers every data word
B. Is completely idle
C. Initiates the transfer and is interrupted after completion
D. Controls memory addressing continuously
Answer: C

7. Which signal is used by DMA controller to request control of the bus?
A. HOLD
B. READY
C. RESET
D. ACK
Answer: A
8. Which signal is sent by CPU to acknowledge DMA request?
A. HOLD
B. HLDA
C. READY
D. INTR
Answer: B

9. DMA improves system performance by
A. Increasing instruction count
B. Reducing interrupt handling
C. Reducing CPU wait time
D. Increasing clock cycle time
Answer: C
10. Which of the following is NOT a DMA transfer mode?
A. Burst mode
B. Cycle stealing mode
C. Transparent mode
D. Polling mode
Answer: D
11. In burst mode DMA
A. CPU and DMA share the bus simultaneously
B. DMA transfers one byte at a time
C. DMA transfers an entire block at once
D. CPU has highest priority
Answer: C
12. Cycle stealing DMA means
A. DMA takes control of the bus permanently
B. DMA steals one CPU cycle per transfer
C. CPU steals cycles from DMA
D. Data transfer occurs only during idle time
Answer: B
13. Transparent DMA occurs when
A. CPU is halted
B. CPU is executing instructions
C. CPU is idle
D. Cache is active
Answer: C
14. Which register holds the starting memory address in DMA?
A. Data register
B. Control register
C. Address register
D. Status register
Answer: C
15. Which register stores the number of bytes to be transferred?
A. Address register
B. Count register
C. Control register
D. Buffer register
Answer: B
16. DMA controller generates
A. Only interrupt signals
B. Memory addresses
C. Instruction codes
D. Clock pulses
Answer: B
17. DMA operation is faster because
A. CPU executes fewer instructions
B. DMA bypasses the CPU

C. Cache is disabled
D. Memory speed increases
Answer: B
18. Which type of interrupt is used after DMA completion?
A. Software interrupt
B. Timer interrupt
C. I/O interrupt
D. Hardware interrupt
Answer: D
19. Which bus does DMA primarily use?
A. Control bus
B. Address bus
C. Data bus
D. All of the above
Answer: D
20. Which device commonly uses DMA?
A. Keyboard
B. Mouse
C. Disk drive
D. Printer
Answer: C
21. DMA reduces
A. Memory access time
B. CPU overhead
C. Instruction execution time
D. Cache misses
Answer: B
22. Which of the following is a disadvantage of DMA?
A. Complex hardware
B. Slower data transfer
C. Higher CPU involvement
D. Increased instruction count
Answer: A
23. In DMA, who becomes the bus master during transfer?
A. CPU
B. Memory
C. I/O device
D. DMA controller
Answer: D
24. Which DMA mode has the least CPU interference?
A. Cycle stealing
B. Burst mode
C. Transparent mode
D. Demand mode
Answer: C
25. Demand mode DMA means
A. DMA transfers only one byte
B. DMA continues transfer until device stops requesting
C. CPU controls transfer
D. DMA transfers during idle time only
Answer: B
26. Which register specifies the type of DMA operation?

A. Address register
B. Count register
C. Control register
D. Status register
Answer: C
27. DMA controller increments
A. Data value
B. Address value
C. Control signal
D. Interrupt count
Answer: B
28. DMA cannot be used for
A. High-speed I/O devices
B. Large block transfers
C. Low-speed I/O devices
D. Small data transfers
Answer: D
29. Which feature allows multiple DMA channels?
A. Interrupt controller
B. Cache memory
C. DMA controller
D. Memory controller
Answer: C
30. DMA transfer ends when
A. CPU stops
B. Count register reaches zero
C. Address register resets
D. Interrupt is disabled
Answer: B
31. Which DMA technique temporarily suspends CPU execution?
A. Transparent mode
B. Cycle stealing
C. Burst mode
D. Demand mode
Answer: C
32. DMA is preferred over interrupt-driven I/O because
A. It uses polling
B. It supports multitasking
C. It reduces CPU load
D. It increases interrupts
Answer: C
33. DMA controller communicates with I/O devices via
A. Registers only
B. Control signals
C. Clock pulses
D. Instruction codes
Answer: B
34. Which DMA register indicates completion status?
A. Address register
B. Count register
C. Status register
D. Data register

Answer: C
35. Which DMA mode allows CPU and DMA to work simultaneously?
A. Burst mode
B. Transparent mode
C. Demand mode
D. Block mode
Answer: B
36. DMA requires which type of addressing?
A. Virtual addressing
B. Logical addressing
C. Physical addressing
D. Relative addressing
Answer: C
37. Which is NOT a benefit of DMA?
A. Faster data transfer
B. Reduced CPU workload
C. Improved multitasking
D. Increased CPU instruction count
Answer: D
38. DMA is most effective when
A. Data size is small
B. CPU speed is low
C. Data size is large
D. Cache is disabled
Answer: C
39. Which protocol ensures bus control transfer in DMA?
A. Handshaking
B. Polling
C. Spooling
D. Buffering
Answer: A
40. After DMA transfer completion
A. CPU continues without notification
B. DMA halts permanently
C. CPU is interrupted
D. Memory is cleared
Answer: C