Daffodil International University

Faculty of Science and Information Technology
Department of CSE
Final Examization **Semester: Summer 2022**
Course Code: CSE 411 (D4) **Course Title: Computer Architecture & Organization**
Sectine: All

Time: 02:00H **[Answer all the Questions. Obtain marks in the right side]** **Full marks: 40**

Question 1 *(CO2, L2)* ***8 Marks***

a. Illustrate the **Block Diagram** and **Basic Operation** of computer system **[2]**

b. Express **Instruction Set Design** by showing example of the **instruction formats** of each design. **[4]**

c. How many types of **Data Operands** used in computer system? Establish **one instruction** from each data operands. **[2]**

Question 2 *(CO3, L3)* ***8 Marks***

a. Prepare the **Alternative Pipeline** for a situation where **instruction 5** is a conditional branch to **instruction 12.** Mention in which time unit the **pipeline is full &** & which instructions are need to be **flashed** from the pipeline. **[2]**

b. Discover **Resource Hazards** and **Data Hazards** with explaining which create more complication. **[3]**

c. Suppose you have **13 instructions** to process with **no-branch.** Assume that the instruction ity uu enters ithoue pipeline is **5 miliseconds.** Now compute the **total time** required for a pipeline with **5 stages** to execute all the instructions and find out the **speedup factor.** **[7]**

Question 3 *(CO3, L3)* ***12 Marks***

a. Predict you have a **Main Memory** which is size of **512 words** and a **Cache Memory** size of **64 words.** Each line of cache memory can hold a **block of & words** at a time. Now sketch the **Direct Mapping** from Cache to Main Memory with exampie of **Address Structure.** Also mention two **advantages and disadvantages** of Direct Mapping. **[8]**

b. Demonstrate the **logical** and **physirat Cache addressing** with figure. **[2]**

c. Show the **Cache operation** overview **[2]**

Question 4 *(CO4, L3&L4)* ***12 Marks***

a. Identify **demand paging. How Virtual** memory ensure **Memory Protection**? **[3]**

b. Discover what **Virtual memory** actually is? Exhibit virtual memory **mapping** with proper diagram. **[5]**

c. Identify that Virtual memory support the **Address Translation**. Relate why it is required to translate address, with the support of proper diagram. **[4]**