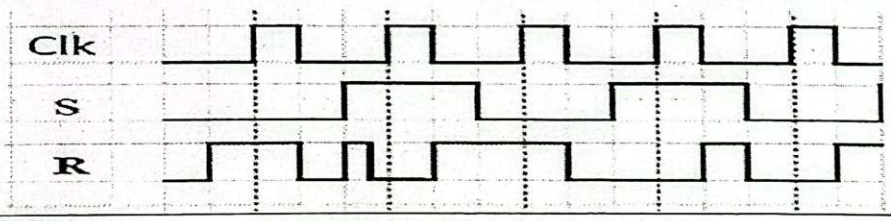
Daffodil International University

Faculty of Science & Information Technology
Department of Computer Science & Engineering
Final Examination, Fall 2025
Course Code: CSE223, Course Title: Digital Logic Design
Level: 2 Term: 2 Batch: 66

Time: 02:00 Hrs **Marks: 40**

Answer ALL Questions

[The figures in the right margin indicate the full marks and corresponding course outcomes. All portions of each question must be answered sequentially.]

1.	*a)*	An automated campus parking gate uses three binary sensors and one control signal: • E: Entry sensor (1 = vehicle entering detected, 0 = none) • X: Exit sensor (1 = vehicle exiting detected, 0 = none) • R: Reserve/override button (1 = Reserve mode active, 0 = normal) • CLK: System clock (edge triggered) Design a **3-bit bidirectional car occupancy counter** (counts current cars in lot) with range **0 to 7** and the following control logic: 1. When **E = 1** and **R = 0**, the counter **increments by 1** on the next clock (vehicle entered). 2. When **X = 1**, the counter **decrements by 1** on the next clock (vehicle exited). If both E and X = 1 simultaneously, they cancel and the count does not change. 3. If the count reaches **7** (full), a **FULL LED** should be ON; further entry attempts (E=1) while at 7 must **not** increase the count. 4. If the count is **0** (empty), an **EMPTY LED** should be ON; further exit attempts (X=1) while at 0 must **not** decrease the count. 5. When **R = 1** (Reserve mode), **no new entries are permitted** — E must be ignored for incrementing; exits still decrement the count. **Tasks:** a) **Build** the **complete truth table / state-action table** covering inputs (E, X, R) and present state (Q2 Q1 Q0) to next state ($Q2^+$ $Q1^+$ $Q0^+$) and outputs (FULL, EMPTY). b) **Choose** a flip-flop type (D or JK or T) and **derive** the flip-flop input equations required to implement the next-state logic. c) **Draw** the **logic circuit diagram** (flip-flops + combinational logic) implementing the counter and FULL / EMPTY indicators. Indicate clocking and any necessary gating for the Reserve input.	**10**	**CO3**
	b)	$F(A,B,C,D)= \sum(0, 1, 4, 5, 9, 10, 14, 15)$ **Implement** the following function using multiplexer, where C, D is input and A, B selector.	**5**	
2.	*a)*	For the positive edge triggered Flip-Flop determine the following output timing diagram Q and Q' with the given state of S, R, and CLK in figure below. The flip-flop is initially in SET state. Now **draw** the timing diagram of Q and Q'. 	**5**	**CO4**

	b)	**State** the difference between latch and flip-flop.	5	
3.	*a)*	A communication system stores data in a 4-bit word 1110, where all four bits are loaded into the flip-flops simultaneously but need to be transmitted one bit at a time to another device. Based on this requirement, apply your understanding to **identify** the type of register suitable for this operation explaining the process. Design block diagram and truth table to illustrate how the bits move through the circuit.	5	
	b)	**Draw** a block diagram 4-bit binary synchronous up counter.	5	
	c)	**Implement** the following Boolean expression using PAL, F1= $\sum$ m (3,5,7) and F2 = $\sum$ m (4,5,7)	5	

Note: You may add or delete rows as per your requirements. Mention CO's in the right side of the table as per your course outline.