



Daffodil International University
Faculty of Science & Information Technology
Department of Software Engineering
Final Examination, Summer 2026

Course Code: SE 213; Course Title: Digital Electronics & Logic design
Sections & Teachers: A-D(SP), E-H(NIR), I(DAT),J-L(SIK),M(KRY),N(MTE),O(KNA),P(FT)

Time: 2 Hours

Marks: 40

Answer **ALL** Questions

[The figures in the right margin indicate the full marks and corresponding course outcomes. All portions of each question must be answered sequentially.]

1.	a)	$F(I, J, K, L) = \sum (5, 6, 7, 8, 9) + \sum d(10, 11, 12, 13, 14, 15)$ Configure k-map simplification technique using don't-care condition to derive the most simplified version of the above expressions along with circuit.	[Marks-5]	CLO-2 Level-3
	b)	Express the following function into Product of Sum (POS) standard canonical form and then convert it into its opposite canonical form. $F(A, B, C) = (A + \bar{B}C)(\bar{A}B + \bar{C})$	[Marks-5]	
2.	a)	Build a full adder logic circuit using decoders.	[Marks-5]	CLO-3 Level-3
	b)	An autonomous bus operates on a route from DSC to Dhanmondi with 10 locations, numbered in descending order from Stop 9 to Destination 0. Stop 9 is nearest to DSC, while Destination 0 is the final stop at Dhanmondi. A priority encoder circuit is required to control the bus stop requests. Two passengers simultaneously request to get off at Stops 8 and 5. Illustrate the priority encoder by deriving the Boolean expressions and determine which passenger's stop request is served first.	[Marks-5]	
	c)	Demonstrate the following Boolean function using an appropriate multiplexer. Show all steps including Implementation table and final design. $F(G, H, I, J) = \sum (0, 3, 5, 6, 8, 9, 14, 15)$	[Marks-5]	
3.	a)	Show the difference between sequential circuit and combinational circuit.	[Marks-3]	CLO-4 Level-3
	b)	T flip flop is a version of the J-K flip flop". Express the following statement with an appropriate circuit diagram.	[Marks-5]	
	c)	i) In 4-bit shift register: 1001, illustrate how many clock pulses are required to change the content of shift register when all 1's (using by XOR gate for last two bit) ii) Draw and describe the block diagram of Serial Input Serial Output (SISO) Register	[Marks-3+4]	