



Daffodil International University
Faculty of Science & Information Technology
Department of Software Engineering
Midterm Examination, Summer 2026
Course Code: SE222; Course Title: Computer Architecture
Sections & Teachers: 45A to 45L (MH, KBB, HKN, FC)

1,000,000

Time: 1 Hour 30 Mins

Marks: 25

Answer ALL Questions

[The figures in the right margin indicate the full marks and corresponding course outcomes. All portions of each question must be answered sequentially.]

1.	a)	A processor operates at 1.8 GHz with the following instruction mix: <table><tr><td>Instruction Type</td><td>Frequency</td><td>CPI</td></tr><tr><td>ALU Operation</td><td>25%</td><td>1</td></tr><tr><td>Floating Point</td><td>20%</td><td>9</td></tr><tr><td>Memory Access</td><td>35%</td><td>4</td></tr><tr><td>Branch</td><td>20%</td><td>3</td></tr></table> Compute the effective CPI, MIPS rate, and Execution Time for a program containing 10 million instructions.	Instruction Type	Frequency	CPI	ALU Operation	25%	1	Floating Point	20%	9	Memory Access	35%	4	Branch	20%	3	[Marks-5]	CLO-1 Level-2																	
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	b)	Explain the function of a General Purpose Processor (GPP) and its instruction patterns with a suitable diagram.	[Marks-4]																																	
	c)	Differentiate the program flow of control without interrupts and with interrupts in a computer system with suitable diagrams.	[Marks-3]																																	
	d)	A database server spends 40% of its execution time on disk I/O operations. A new SSD upgrade makes the disk I/O portion 6 times faster. Analyze the overall system speedup using Amdahl's Law and state whether the upgrade provides a significant performance gain.	[Marks-3]																																	
2.	a)	Analyze the execution steps of the Hypothetical Processor for the given scenario. <table><tr><td colspan="2">Memory</td><td colspan="2">CPU Register</td></tr><tr><td>400</td><td>1808</td><td>PC</td><td>400</td></tr><tr><td>401</td><td>6809</td><td>AC</td><td>0000</td></tr><tr><td>402</td><td>580A</td><td>IR</td><td>—</td></tr><tr><td>403</td><td>480B</td><td></td><td></td></tr></table> Here memory contents are represented in hexadecimal <table><tr><td>808</td><td>0012</td><td></td></tr><tr><td>809</td><td>0006</td><td></td></tr><tr><td>80A</td><td>0004</td><td></td></tr><tr><td>80B</td><td>0000</td><td></td></tr></table> Opcode: 0001—Load AC from Memory, 0110—Add AC from Memory, 0101—Subtract AC from Memory, 0100—Store AC to Memory	Memory		CPU Register		400	1808	PC	400	401	6809	AC	0000	402	580A	IR	—	403	480B			808	0012		809	0006		80A	0004		80B	0000		[Marks-4]	CLO-2 Level-4
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	b)	Distinguish between the levels of the memory hierarchy in terms of speed, cost, and capacity, and why using a single large fast memory is impractical for modern computer systems.	[Marks-3]	
RAM -RW D-RW DVD-RAM	c)	Examine the role of tag, line, and word fields in cache address decomposition and how the processor determines a <u>cache hit</u> or miss during a memory read operation.	[Marks-3]	