



Daffodil International University

Department of Software Engineering
Faculty of Science & Information Technology
Final Examination, Fall 2025

Course Code: SE 222; Course Title: Computer Architecture
Batch & Sections: 43 (A to O)

Course Teachers: SR, AS, FBR, HKN

Time: 2:00 Hrs

Marks: 40

Answer ALL Questions

[The figures in the right margin indicate the full marks and corresponding course outcomes. All portions of each question must be answered sequentially.]

1.	a)	Analyze how set-associative mapping reduces the limitations found in direct-mapped caches and associative-mapped caches.	[Marks-5]	CLO-2 Level-4	
	b)	Consider a direct mapped cache that has a physical address of 16 bits and among them 4 bits is for tag. Memory block size is of 32 bytes. Examine Main memory size, Cache size and no of blocks in memory.	[Marks-5]		
2.	a)	Illustrate the steps of Booth's algorithm for 2's complement multiplication for the following values: (Using 4 bits). Multiplicand: -4 Multiplier: -6	[Marks-6]	CLO-3 Level-4	
	b)	Explain user-visible registers and flag register.	[Marks-5]		
	c)	Articulate zero, one and two address machine instructions with example.	[Marks-3]		
	d)	Transform the following IEEE-754 32 bit floating point binary numbers into decimal. <table border="1"> <tr> <td>0</td> <td>01111100</td> <td>111000000000000000000000</td> </tr> </table>	0		01111100
0	01111100	111000000000000000000000			
3.	a)	Visualize a Five-stage pipelining process for 6 instructions and discuss about how it improves execution time over non-pipelined execution process.	[Marks-4]	CLO-4 Level-3	
	b)	Show the Effective Address (EA) calculation process of Indirect, Register Indirect and Displacement addressing technique with figure.	[Marks-3]		
	c)	Investigate the factors that may limit the performance of pipelining process.	[Marks-3]		