

Digital Logic Design Quiz 4 Section: 65_E Spring 2025		
1.	Draw the diagram and truth table of a. Controlled D Latch b. JK Flip-Flop c. SR Latch	[4+4+3=11]
2.	Draw the <u>figure</u> and <u>timing diagram</u> of a 2-bit asynchronous down counter.	[4]

*This is not the actual question file. We got the image but not in good condition. So, re-written in this file.