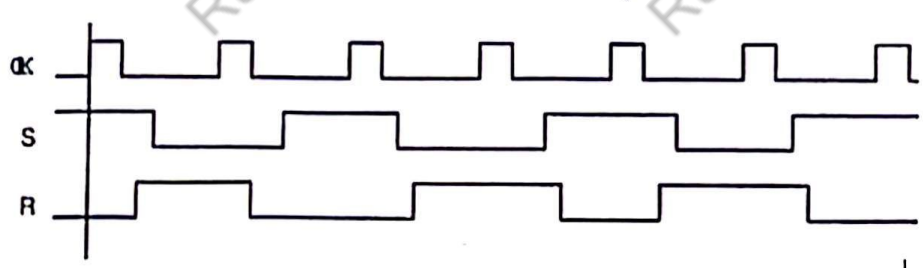
Daffodil International University

Department of Computer Science and Engineering
Faculty of Science & Information Technology
Final Examination, Fall 2022
Course Code: 223, Course Title: Digital Electronics
Level: 2 Term: 2 Batch: 59

Time: 02:00 Hrs **Marks: 40**

Answer ALL Questions

1.	*a)*	A global electrical juncture is now occurring. We must save power in order to get out from this circumstances. You need to develop a system to diminish the amount of power used in your home. Imagine that you had a television, fan, air conditioner, and light in your home, but you can only use two of these at once. Now develop truth table, Boolean expression and circuit for the system.	[10]	CO2
2.	*a)*	Construct 4 to 16 line decoder with four 2 to 4 line decoder.	[5]	CO3
	b)	Construct 4 to 2 line Priority Encoder where I_3 holds top priority.	[5]	
	c)	Implement the following Boolean function with a multiplexer. $F(A, B, C, D) = \sum (0, 2, 4, 5, 8, 10, 11, 14)$	[5]	
3.	*a)*	Compare sequential circuit and combinational circuit.	[5]	CO4
	b)	Determine the output states Q and Q' for S-R flip flop, given the following pulse inputs. 	[10]	

Daffodil International University

Department of Computer Science and Engineering
Faculty of Science & Information Technology
Final Examination, Spring 2022
Course Code: CSE223/212 (Day), Course Title: Digital Electronics
Sections, Teachers: All

Time: 2:00 Hrs **Marks: 40**

Answer ALL Questions

[The figures in the right margin indicate the full marks and corresponding course outcomes. All portions of each question must be answered sequentially.]

1. Suppose you need to implement a traffic control system for a four junction point road. Where only one signal will be open at a time and the others will be remain closed. Traffic signal will be changed automatically for specific combination. Now **Explain and build** a truth table, Boolean expression and circuit for this scenario. **[10]** **CO2**

2. *a)* To perform a lab task you need to implement a two bit binary adder. In this case you will have to use Decoder along with other basic logic gates. **Demonstrate** the block diagram for adding two bit binary number $X_1 X_0$ and $Y_1 Y_0$. **[5]** **CO3**

b) **Construct** 4 to 11 Decoder with proper documentation. **[5]**

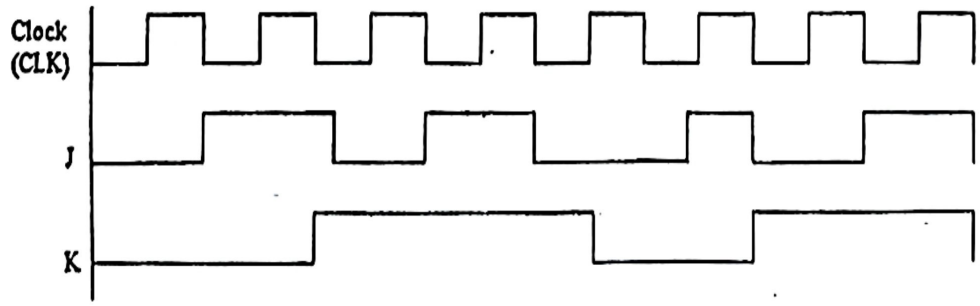
c) **Analyze** the following function using 4x1 multiplexer where A and B are considered as selectors. **[5]**

$$F(A, B, C, D) = \Sigma(1, 3, 4, 5, 6, 7, 12, 14)$$

d) **Develop** an 8 to 3-line Encoder with a priority list. **[5]**

3. *a)* **Define** S-R latch with NOR gate. **[5]** **CO4**

b) **Identify** the output states Q and Q' of J-K flip flop for the following input pulse: **[5]**



Daffodil International University

Department of Computer Science and Engineering

Faculty of Science & Information Technology

Final Exam Examination, Summer 2020 @ DIU Blended Learning Center

Course Code: CSE223 (Day/Evening), Course Title: Digital Electronics

Level: 2 Term: 2 Section: ALL

Instructor: ALL Modality: Open Book Exam

Date: 20 August, 2020 Time: 09:00-01:00pm

Four hours (4:00) to support online open/case study based assessment Marks: 40

Directions:

- **Students need to go through the CASE STUDY shown in this exam paper.**
- **Analyze and answer specific section based on your own thinking and work.**
- **Do not share as this will be treated as plagiarism by Blended Learning Center.**

Answer any questions

1. Design a digital logic circuit for 2-bit binary numbers X and Y using decoder. The outputs are A, B, and C, where A is 1 if X>Y, B is 1 if X=Y, and C is 1 if X<Y. 5

2. In digital electronics lab class you face a problem, that there is no binary adder in lab room to add two binary numbers. However, it is necessary to immediately solve one of your experiments using binary adder. In this time, you find 2 to 4 decoders. Is it possible to get binary adder within a short time? 5

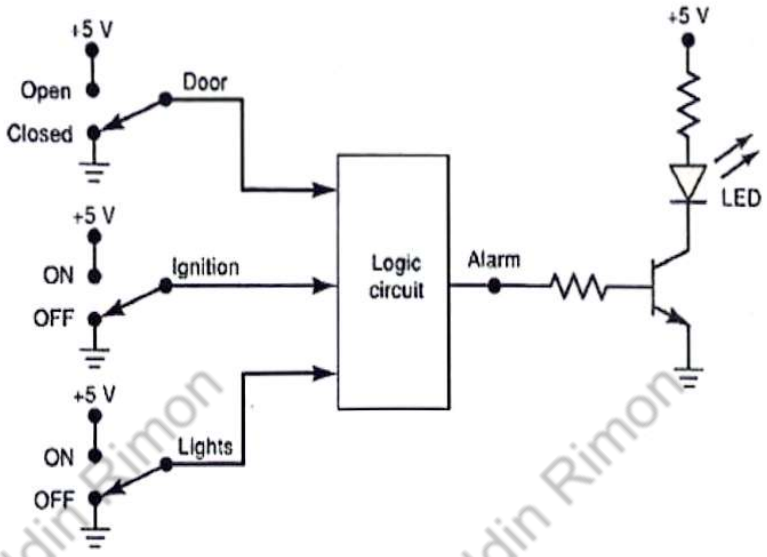
3. Suppose you have a six-lane highway connected with a bridge over the Padma river. Only one lane can use the bridge at a particular time. Now as an engineer you need to design a circuit that will control the cars from the 6 lanes using the bridge one after another. 5

4. Implement the following function using 4x1 multiplexer where C and D are considered as a selector. 5

$$F(A, B, C, D) = \Sigma(0, 2, 4, 5, 7, 8, 10, 12, 15)$$

5. You have 3 LED lights: Red (R), Green (G), and Blue (B) along with one control panel for multiple inputs. You need to design a circuit to make the LED light on. However, for every single input it is not required to turn on the LED light. On the other hand, it is also possible to turn on two or three lights at a time. How can you achieve this circuit using a familiar concept of combinational logic circuit? 5

6. The following diagram to present a smart vehicle alarm circuit used to detect certain undesirable situations. The 3 switches are used to indicate the status of the door by the driver's seat, the ignition and the lights. Design a logic circuit with 3 switches as inputs, so that the alarm will be activated whenever either of the following conditions occurs- 5



a. The lights are off while the ignition is on.
b. The door is open while the ignition in on.

7. Ms. Marry, a successful business woman. She is extremely interested with modern technology and wants to make an IOT based smart home system. With the help of this system she will be able to manage different devices using a single remote controller system. In her smart home system, she needs to control a LED TV, an Air Conditioning System, a DVD Player, and a CCTV Camera. How can you help Ms. Marry to make this smart home system using a combinational logic circuit? Explain your opinion with proper documentations. 10

Daffodil International University

Department of Computer Science & Engineering
Faculty of Science & Information Technology
Final Examination Semester: Summer 2019
Course Code: CSE 212 Course Title: Digital Electronics
Batch: Day Section: All

Time: 2.0 hours **Full Marks: 40**

Answer any four(04) from the following questions

QUESTION 1: [10.0]

a) Suppose there are two numbers $X_0X_1X_2X_3$ and $Y_0Y_1Y_2Y_3$. Construct a circuit that will produce the BCD summation of these two numbers. Describe your answer with proper truth table. [7]

b) One feature that has made J-K flip-flop more efficient that SR flip-flop- what is it and draw the diagram of J-K flip-flop. [3]

QUESTION 2: [10.0]

a) A circuit which works both as an adder and a subtractor- draw the circuit diagram and explain its operation. [6]

b) Implement a full adder circuit using multiplexers. [4]

QUESTION 3: [10.0]

a) Is it possible to construct an 8 to 1 MUX using 4 to 1 MUX? If so please draw the diagram. [4]

b) Suppose you want to store the output of a 2-bit Full adder. Which circuit are you going to use- show it in a diagram? [4]

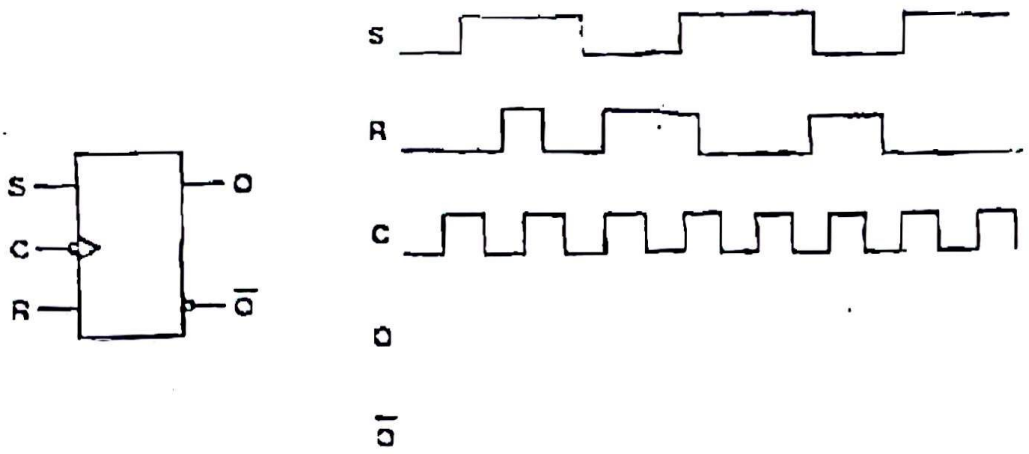
c) Differentiate between latch and flip-flops. [2]

QUESTION 4: [10.0]

a) How can a decoder be used as a demultiplexer? Justify your answer with proper diagram. [4]

b) Implement a D FF using JK FF.

c) Determine the output states for the Clocked S-R Flip-Flop, given the following pulse inputs :



QUESTION 5: [10.0]

a) Implement the following function with a multiplexer: [6]

$$F(W, X, Y, Z) = \Sigma(1, 3, 4, 11, 12, 13, 14, 15)$$

b) Find out True/False:

i. Asynchronous inputs affect the state of the FF independent of the clock. [4]

ii. A MUX is known as data distributor.

iii. An edge-triggered FF changes state always at the beginning.

iv. Decoders are used in Input/Output selection in computers.

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Department of Computer Science & Engineering
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Final Examination Semester: Fall 2019
Course Code: CSE 212(Day) Course Title: Digital Electronics

Time: 2.0 hours **Full Marks: 40**

Answer any four(04) from the following questions

1. a) Suppose you have adders and some normal gates in your lab and your teacher asked you to construct a binary adder and subtractor in one circuit. How would you design it and explain its operation. 5

   b) Suppose you have J-K flip-flop in your lab and you want to construct a D flip-flop from it. How can you design it? 3

   c) Write down the differences between NAND and NOR latch. 2

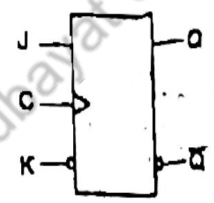
2. a) Construct a 2 to 4 decoder with its truth table and draw a circuit which stores its output in one clock signal. 6

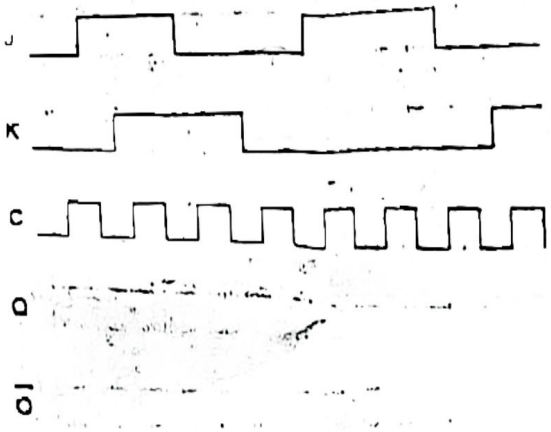
   b) Implement a full adder circuit using multiplexers. 4

3 a) Construct a 4 to 16 decoder using 3 to 8 decoders and explain how it works? 5

   b) Differentiate between encoder and priority encoder. Explain the basic operation of priority encoder. 5

4. a) Determine the output states for the J-K flip flop, given the following pulse inputs; consider initial ouput is zero : 3





b) Find out True/False: 5

I. Asynchronous inputs affect the state of the FF independent of the clock.
II. A MUX is known as data distributor.
III. An edge-triggered FF changes state always at the beginning.
IV. Decoders are used in Input/Output selection in computers.
V. JK flip-flop has an ambiguity.

c) What is the output of an XOR gate when a logic signal and its exact inverse are connected to its inputs? 2

5. a) Implement the following function with a multiplexer: 5

$$F(W, X, Y, Z) = \sum(0, 1, 3, 4, 8, 9, 15)$$

b) Simplify the following Boolean function : 5

$$F(A, B, C, D) = \Sigma(1, 3, 7, 11, 15) + d\,\Sigma(0, 2, 5)$$